ITRES RESEARCH LIMITED

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DESIGN AND CONSTRUCTION OF A PROTOTYPE POSITION-SENSITIVE X-RAY DETECTOR

FINAL REPORT

prepared by

ITRES Research Limited
Calgary, Alberta

for

The Canada Centre
For Mineral and Energy Technology

MICROMEDIA

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1. SUMMARY

A position-sensitive x-ray detector based on the EEV P8602 CCD array sensor has been designed and fabricated. The detector assembly incorporates a single-stage thermoelectric cooler and water-cooled heat sink. The sensor has an active area of 8.5 x 12.8 mm, with a minimum clearance on the long dimension of 3.3 mm on the side nearest the x-ray tube. It consists of an array of 385 x 576 individual sensors (pixels), each of which can be read out on its own or combined with row and/or column neighbors.

With water cooling of the heat sink to 27°, the temperature of the CCD during normal operation can be maintained at 0° with the present design, but lower temperatures should be achievable with a more powerful thermoelectric cooler.

Noise performance of the ITRES test readout system has been reduced to the point where individual x-ray events should be detectable; however, basic tests show that individual x-ray pulses of the expected magnitude are not observed, apparently due to charge spreading in the readout process. Some charge spreading is inherent in the chip when x-rays are absorbed outside the depletion region, but the amount of spreading observed is larger than that attributable to this effect.

In conclusion we believe that a commercially viable detector and readout system can be developed for incorporation into the EMR stress diffractometer, although further work is needed to determine the cause of the small amplitude observed for the x-ray pulses and to determine the optimum operating mode. Efforts should also be made to obtain arrays with larger depletion thicknesses, as reported in the literature.

A commercial dual-detector subsystem, excluding the host computer which would probably be an IBM PC, could be manufactured for a cost

in the $25,000 range (small quantities). Development costs, estimated to be in the $100,000 range; marketing costs and profit are not included in the above figure. These costs are based on assumptions about the feasibility of a simplified approach to the design. The validity of these assumptions needs to be tested before committing to this approach.

2. INTRODUCTION

ITRES contracted with EMR to design and build a prototype positon-sensitive detector for x-rays in the 6-10 keV region, based on present state-of-the-art array sensor technology. The objective was to determine whether solid state array sensors offered a viable alternative to the proportional counters currently used by EMR in stress defractometers.

The contract work was to proceed in three phases, the first consisting on a survey of available linear and two-dimensional array sensors. The second phase involved an evaluation of a selected sensor based on the results of Phase 1 along with a detailed design of the detector system, and the third phase consisted of building and testing an actual detector.

The survey showed that two dimensional CCD array sensors were clearly superior to everything but the Reticon large-area linear arrays. Cooling and temperature stability requirements were relatively severe for the Reticon, and, in spite of the smaller-than-desired length of the available CCD array sensors, it was decided to proceed with evaluation of the EEV P8602 CCD array.

Evaluation of the P8602 using the ITRES test system and an Fe(55) radioactive source revealed a number of problems arising from excess readout noise in the electronics and from dark current and its pixel-to-pixel variations. An accounting for the various noise sources

indicated that the system should be capable of detecting individual x-rays. On the basis of this it was decided to proceed with fabrication of a thermoelectrically cooled detector assembly, consisting of a CCD, a custom board to which it is mounted, a copper block and thermoelectric cooler and heat sink, and an integral preamplifier assembly with the appropriate connectors and cables.

Assembly and basic testing of the detector system is complete. This report documents Phase 3 activities and the observed performance of the detector system.

3. PHASE 3 ACTIVITIES

The detector assembly was fabricated according to the plans in Appendix A. One CCD cracked under pressure applied to it during bonding to the thermoelectric cooler. A second CCD was bonded successfully. The original heat sink proved to be inadequate to dissipate the heat generated by the thermoelectric cooler at normal currents. An improved heat sink with larger dissipating arc was designed, fabricated, and installed.

The larger heat sink was still inadequate, and a simple water circulating system was installed to cool the heat sink. With this change stable, CCD temperatures in the 0°C range were attained, with the heat sink running at 27°C.

A concerted effort to diagnose and improve the noise performance of the ITRES CCD test system resulted in several improvements which brought the readout noise down to about 250 electrons. In addition, the main contributor to the readout noise was determined to be a defective 12 bit A-D converter. We had a great deal of difficulty with the supplies

of this high speed converter, but a replacement unit was eventually obtained and installed. Preliminary tests indicate that instability problems have been cured.

New software was developed to permit accumulation of data rapidly from a single pixel for a sequence of frames. The resulting histograms are free from pixel-to-pixel variations, and short exposures keep the dark current very low. Results using this technique will provide a baseline for evaluation of readout schemes which involve collecting data from all of the pixels in the array.

At the achieved readout noise levels, individual x-ray events should stand out on short exposure histograms. Indications are that, even though the array appears to be collecting the expected amount of charge from individual x-ray events, the charge appears to be spread over several pixels, ruling out straight forward detection of individual events. Further testing is needed to determine the cause of this discrepancy.

4. RESULTS

Results of the design and evaluation effort described in the Phase 1 and 2 reports, together with the work described in Section 3 and in Appendices A and B, demonstrate that a detector of potential usefulness in the EMR stress diffractometer has been completed. The prototype delivered to EMR warrants further tests and evaluation to determine the best operating mode (see Section 5) and to confirm that it has adequate sensitivity and resolution. In connection with this, the reasons for the apparent charge spreading need to be understood, and it is hoped, corrected. Encouragement in the expectation that good performance can be achieved can be derived from the fact that x-ray astronomers have evaluated the same EEV array and obtained, using a much slower readout

system, x-ray pulse height resoultions of 135 ev at x-ray energies in the 1-5 keV range. (D.H. Lamb, f.k. Knight, and D.A. Schwartz, Maximization of X-ray Energy REsolution in GEC CCDs, Harvard-Smithsonian Center for Astrophysics, Preprint Series No. 2131, March, 1985).

5. RECOMMODATIONS FOR FUTURE WORK

Further systematic testing and evaluation of the x-ray detection system is needed before the performance can be understood and a decision made about whether to proceed with evaluation of the unit in an actual diffractometer. These tests are aimed at two major goals:

1) To understand and determine what is needed to eliminate or minimize the apparent charge spreading which is impeding efforts to detect individual x-ray events.

2) To provide a basis for determining the design approach to be employed in developing a commercial version of the x-ray detection subsystem.

The proposed test program consists of the following sequence:

A. SYSTEM TESTS

1. Dark frame analysis, feasibility and usefulness of dark frame subtraction.

2. Tests of new A-D converter to evaluate its performance and contributions to overall system noise. Includes evaluation of effects of increasing analog amplifier gain in order to provide a higher input singal to the A-D converter.

3. Charge transfer tests using collimated light source and pinhole to produce a very small light spot and using both digitized values and oscilloscope to inspect output.

4. Analysis of single pixel outputs from different regions of the array (including storage region) under x-ray illumination.

B. FRAME DATA TESTS

1. Collect blocks of data under x-ray illumination, subtract averaged dark frames, and examine results
   a) via printout of digitized values
   b) via histograms of pixel outputs
   c) via program selection of individual events
2. Same as B1, except do on-chip charge summation prior to readout
   a) vertical summation only
   b) horizontal summation only
   c) rectangular block summation of various sizes, including large blocks representative of proposed readout scheme for commercial unit.

C. X-RAY MODULE TEMPERATURE CORADIENT EVALUATION

1. Obtain dark current average values for nine evenly spaced (including storage region) blocks on the CCD under normal stable cooling conditions.
2. Same as C1 except with a hot surface representative of the X-ray tube adjacent to the open side of the detector assembly.
3. Determine CCD and heat sink temperatures as a function of thermoelectric cooler current and compare with CCD test chamber cooler performance.

APPENDIX A

X-RAY DETECTOR ASSEMBLY

FABRICATION DETAILS

This appendix describes the CCD x-ray detector assembly and its connection to clock and bias signals (EEV part number P8602 s/u). A brief description of the video preamplifier is also provided.

CCD PRINTED CIRCUIT BOARD

The CCD board is a perforated epoxy board; layout of components is shown in Figure 1. Figure 2 shows the schematic for the CCD board.

Contained on this board are static protection resistors (R5a-g, R4, R6) for the clock signals, output reset pulse (ØR) and reset transistor drain (VRD). Resistor R1 is for current limiting in the event of a failure in one of the charge injection diodes connected to TP1 or TP4. The recommended output load resistance (R2, R3) for DOS and OS is 3.3k ohms. The D.C. level for the output gate (OG) is set using resistor R7.

Both the outputs of the CCD array are A.C. coupled to remove the D.C. level, capacitors C3 and C4. Two other capacitors are used to elmiinate noise.

Filtered +15 and -15 volts are obtained from the video preamplifier board.

VIDEO PREAMPLIFIER BOARD

The video preamplifier board uses a printed circuit board, Figure 3 shows the layout of components. Schematic diagram for the video preamplifier is shown in Figure 4.

Video and dummy output signals are jumpered from the CCD board to the video preamplifier. The dummy output is then subtracted from the video output and

a gain of 5 is applied to the result. This is accomplished by using a differential high speed op amp configuration. Resistor R7 is used to optimize the cancellation of clock feed through. The offset adjust R3 is used to place the reset level at 0.0 volts.

The +15 and -15 volt supplies are brought in by the ribbon cable from the CDB-ASC2 (clock driver board - analog signal chain #2). The video output signal BVID, is then taken off of the video preamplifier board by coax cable.

COLD FINGER

The CCD is epoxied into the saddle of the cold finger using thermal epoxy. Figure 5 and 6 show the dimensions of the cold finger. Note: Cold finger is made of ordinary, not OFHC, copper.

THERMAL ELECTRIC COOLER

The thermo-electric cooler is then epoxied to the bottom of the cold finger. Table 1 lists the specifications of the thermo-electric cooler (Melcor Part Number FC-0.7-32-05L).

WATER COOLING

Water cooling was accomplished by inserting a "U" shaped copper pipe into the heat sink. Thermal epoxy was used to secure the copper pipe into the heat sink.

PACKAGING

The 2 printed circuit boards are connected in a 90° configuration as shown in Figure 7. The area within the boundaries of the 2 printed circuit boards is mainly for mounting of a large heat sink.

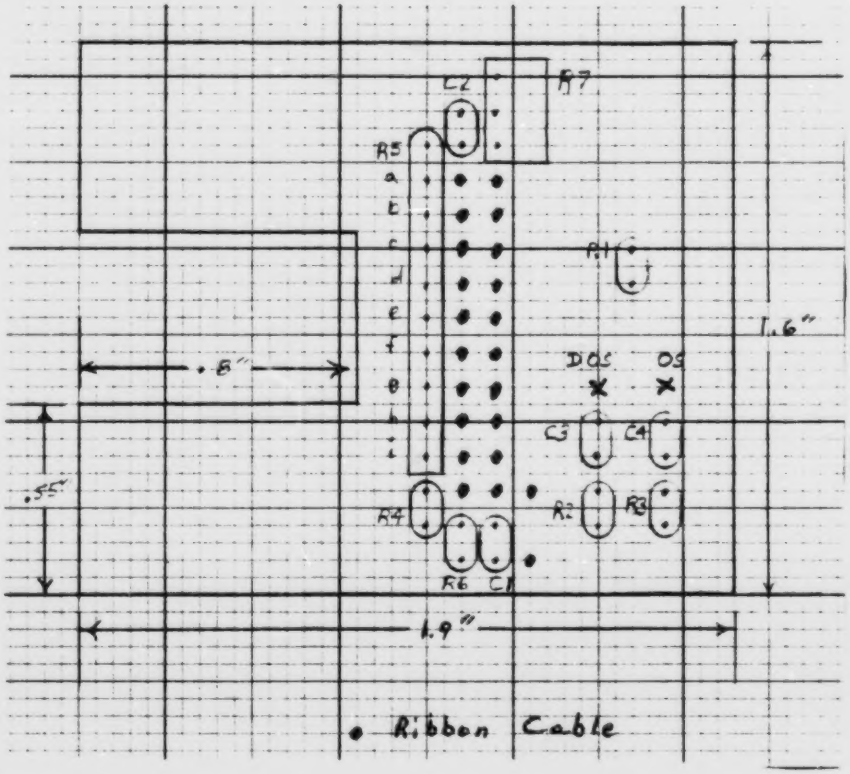
RECOMMENDATIONS FOR FUTURE DETECTOR ASSEMBLIES

- attempt mounting a thermo-electric cooler with a larger cold surface directly to the back of the CCD.
- custom printed circuit baords.
- custom package and insulation.

Figure 1

J.W.S.
10/04/95

X-ray CCD board
(component layout)



2:1 scale

Figure 2

X-ray CCI board
(schematic)

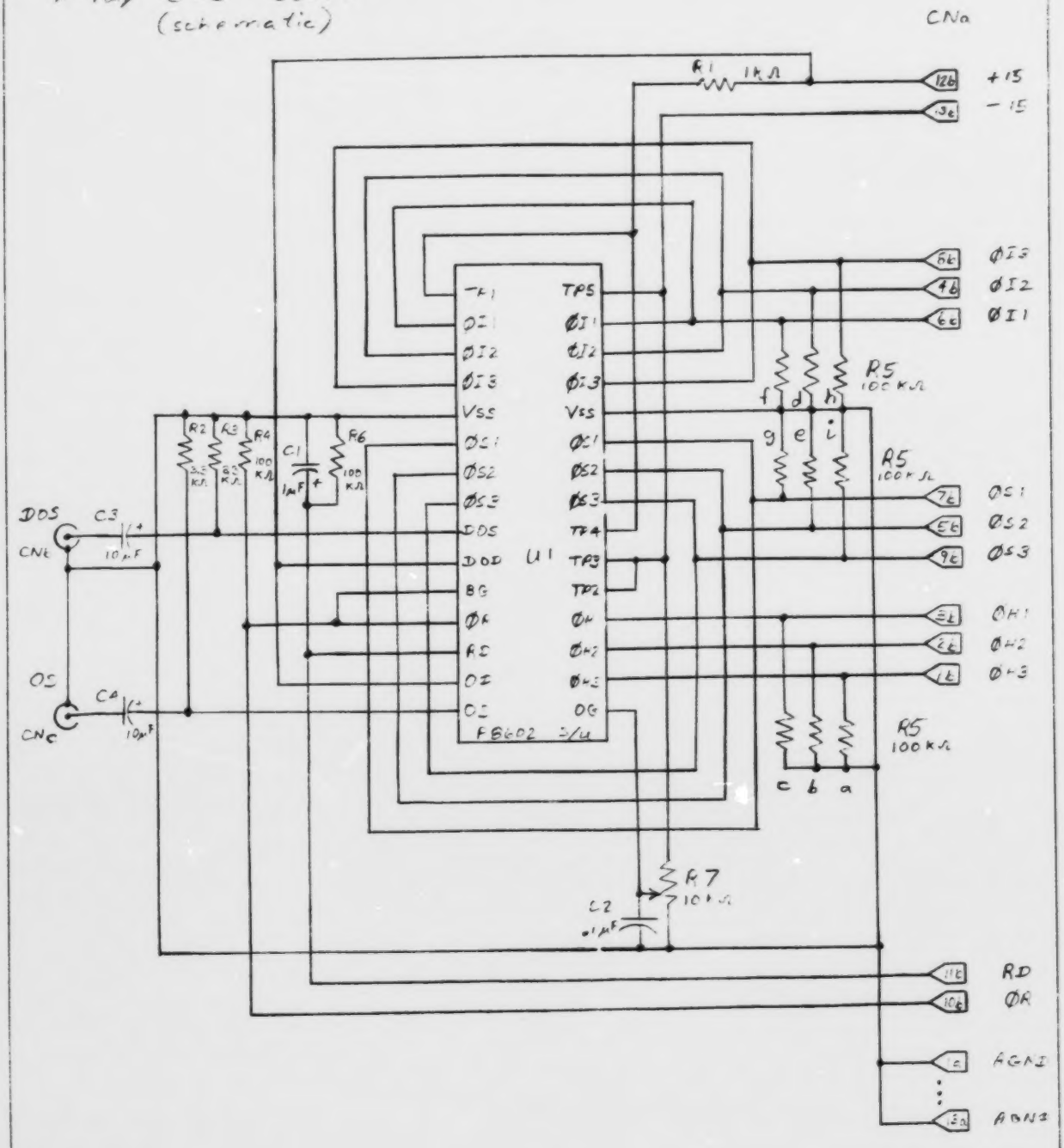
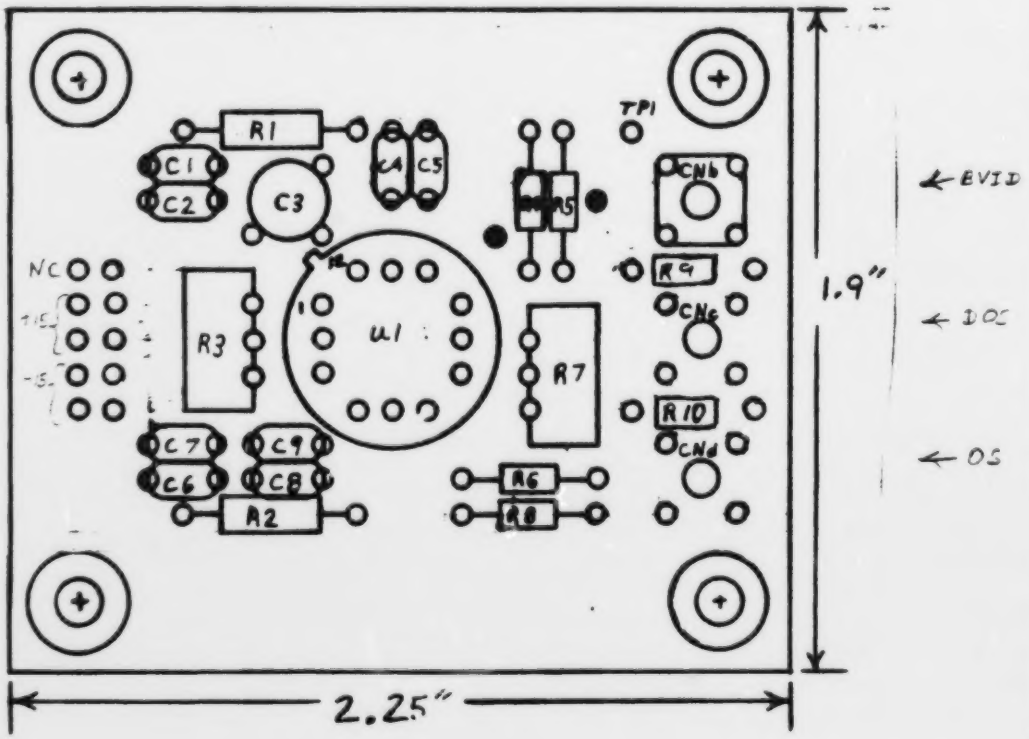


Figure 3

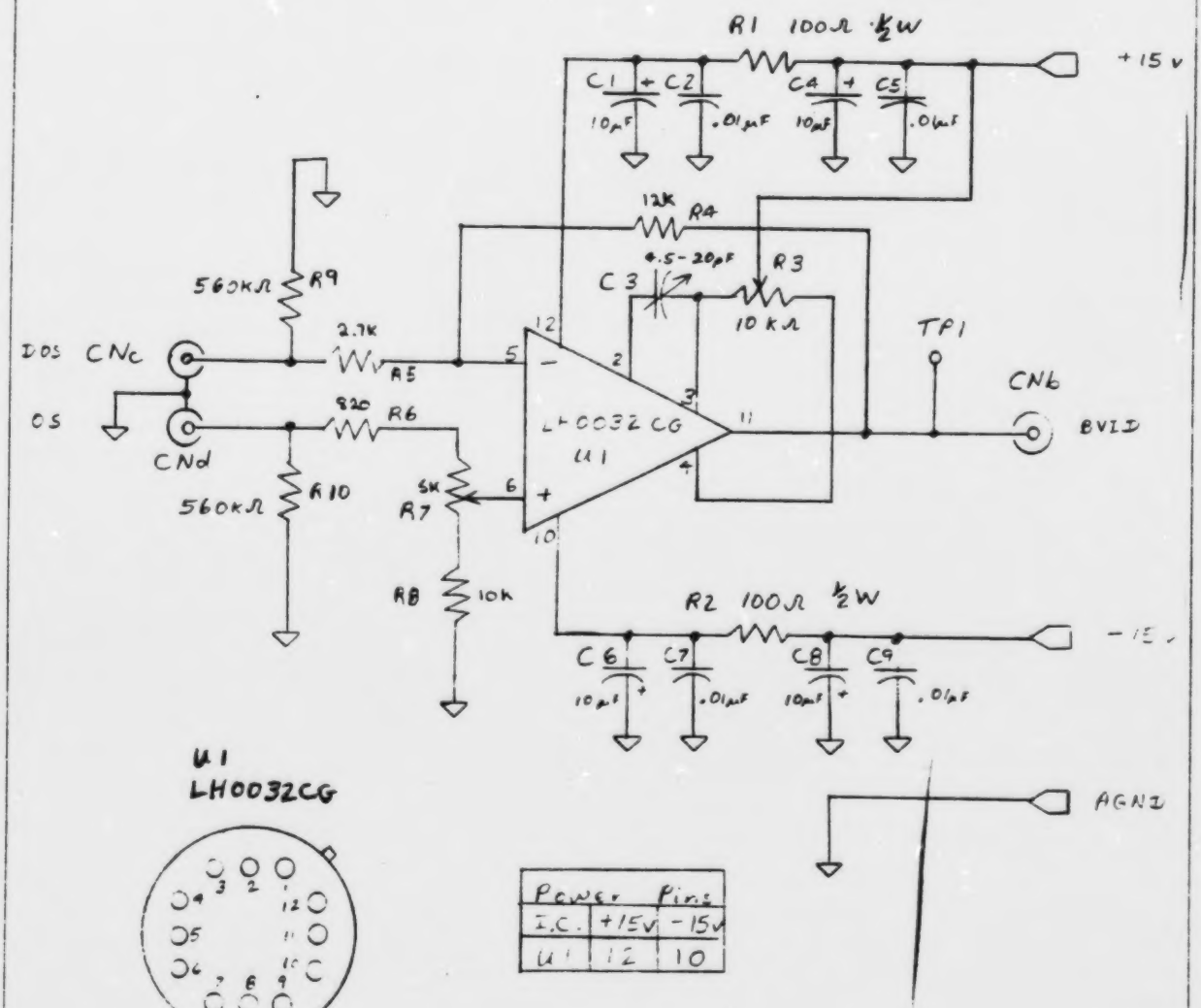
X-ray Video preamplifier board
(component layout)



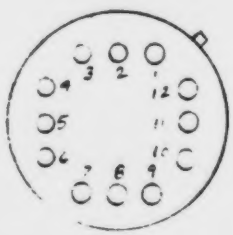
2 : 1 scale

Figure 4

X-ray video preamplifier board (schematic)



U1
LH0032CG



Top View

Power Pins		
I.C.	+15v	-15v
U1	12	10

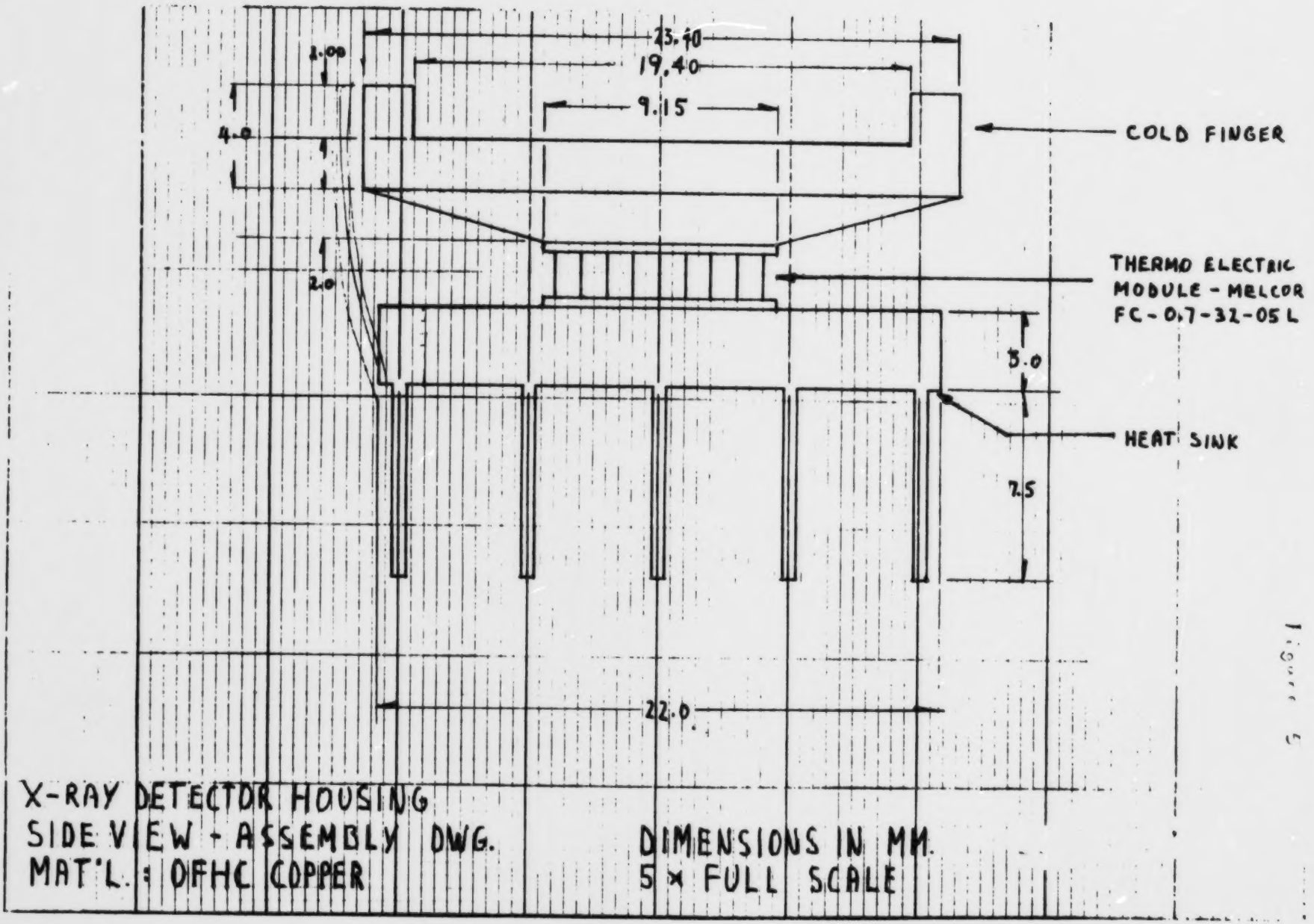

23.40
19.40
9.15
1.00
4.0
2.0
COLD FINGER
THERMO ELECTRIC
MODULE - MELCOR
FC-0.7-32-05 L
3.0
HEAT SINK
7.5
22.0
X-RAY DETECTOR HOUSING
SIDE VIEW + ASSEMBLY DWG.
MAT'L. : OFHC COPPER
DIMENSIONS IN MM.
5 × FULL SCALE

Figure 5

Figure 6

X-RAY DETECTOR HOUSING - COLD FINGER
DIMENSIONS IN MM. - 5 × FULL SCALE
MATL.: OFHC COPPER

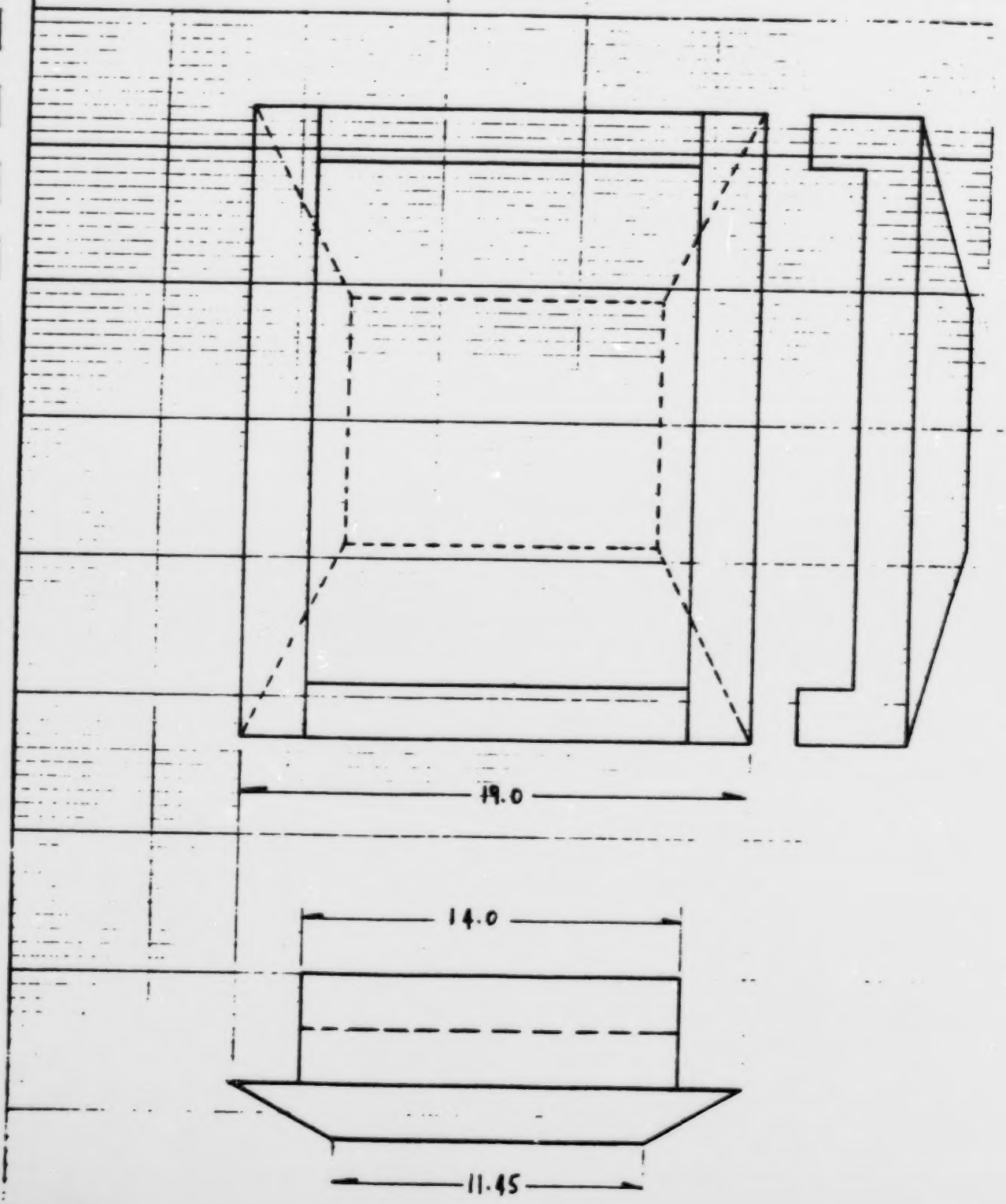
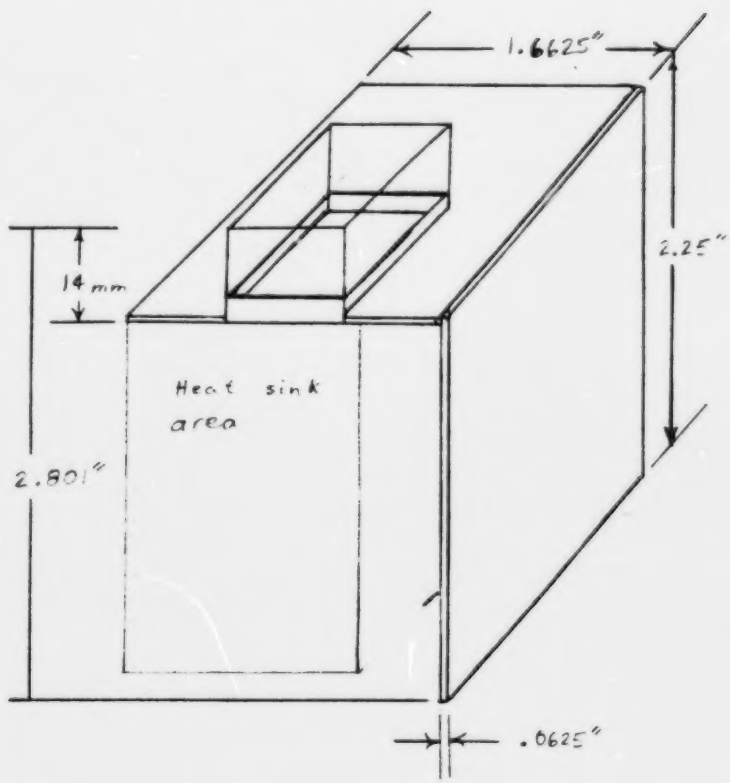


Figure 7

...ry board assembly



1 mm = .03937"

Table 1

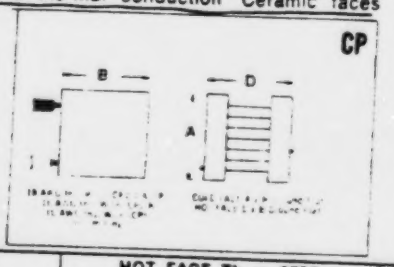
MELCOR
MATERIALS ELECTRONIC PRODUCTS CORP.
994 SPRUCE STREET
TRENTON, NEW JERSEY 08648 U.S.A.
TELEPHONE (609) 393-4178 / TELEX 843314

SOLID STATE COOLING WITH THERMOELECTRICS

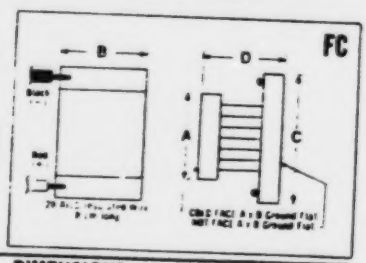
THERMOELECTRIC (PELTIER) HEAT PUMP MODULE SPECIFICATIONS

Thermocouples constructed of N & P elements of highest grade bismuth telluride in form of oriented polycrystalline ingots. Ingot ends soldered to copper bus bars interfaced with ceramic plates, affording good mechanical integrity, high dielectric strength and thermal conduction. Ceramic faces lapped flat (designated Type L) for mechanical interfacing (compression) with heat exchangers. Solderable hot face available on special order, specify Type TL. Temperature Range, −150°C to +110°C. Solid state construction.

CP SERIES



FC SERIES



CATALOG NUMBER	I MAX. AMPS	HOT FACE Th = 27°C Q MAX. WATTS	V MAX. VOLTS	ΔT MAX. °C	MULTIPLIER Q & V	DIMENSIONS MM A	B	C	D	WEIGHT GMS
CP SERIES										
CP 1.0- 7-06L	3.0	1.5	0.85	67.5	0.06	7.5	7.5		3.8	1.5
CP 1.0-14-06L	3.0	2.9	1.70	67.5	0.11	9.2	11.0		3.8	2.1
CP 1.0-31-06L	3.0	6.5	4.75	67.5	0.24	15.0	15.0		3.8	3.8
CP 1.0-63-06L	3.0	13.2	7.62	67.5	0.50	15.0	30.0		3.8	6.4
CP 1.0-127-06L	3.0	26.6	15.0	67.5	1.00	30.0	30.0		3.8	12.0
CP 1.0-127-05L	3.6	32.0	15.0	67.5	1.00	30.0	30.0		3.2	11.3
CP 1.4- 3-10L	3.6	0.8	0.36	70.0	0.04	5.0	10.0		4.8	0.6
CP 1.4- 7-10L	3.6	1.9	0.85	70.0	0.10	10.0	10.0		4.8	1.4
CP 1.4-11-10L	3.6	2.9	1.33	70.0	0.15	10.0	15.0		4.8	2.2
CP 1.4-17-10L	3.6	4.6	2.06	70.0	0.24	15.0	15.0		4.8	3.4
CP 1.4-31-10L	3.6	8.3	3.75	70.0	0.44	20.0	20.0		4.8	6.4
CP 1.4-71-10L	3.6	19.0	8.60	70.0	1.00	30.0	30.0		4.8	14.2
CP 1.4-127-10L	3.6	34.0	15.0	70.0	1.80	40.0	40.0		4.8	25.4
CP 1.4- 3-06L	6.0	1.3	0.36	67.5	0.04	5.0	10.0		3.8	0.5
CP 1.4- 7-06L	6.0	3.0	0.85	67.5	0.10	10.0	10.0		3.8	1.2
CP 1.4-11-06L	6.0	4.6	1.33	67.5	0.15	10.0	15.0		3.8	1.8
CP 1.4-17-06L	6.0	7.2	2.06	67.5	0.24	15.0	15.0		3.8	2.9
CP 1.4-31-06L	6.0	13.0	3.75	67.5	0.44	20.0	20.0		3.8	5.5
CP 1.4-71-06L	6.0	30.0	8.60	67.5	1.00	30.0	30.0		3.8	12.2
CP 1.4-127-06L	6.0	53.6	15.4	67.5	1.80	40.0	40.0		3.8	21.8
CP 1.4-127-045L	8.5	72.0	15.0	67.5	1.00	40.0	40.0		3.3	20.0
CP 2 - 3-10L	8.5	1.8	0.36	70.0	0.10	8.0	15.0		5.7	1.9
CP 2 - 7-10L	8.5	4.3	0.85	70.0	0.23	15.0	15.0		5.7	4.3
CP 2 -15-10L	8.5	9.2	1.81	70.0	0.48	15.0	30.0		5.7	8.9
CP 2 -31-10L	8.5	19.0	3.75	70.0	1.00	30.0	30.0		5.7	18.5
CP 2 - 3-06L	14.0	2.9	0.36	67.5	0.10	8.0	15.0		4.7	1.8
CP 2 - 7-06L	14.0	6.8	0.85	67.5	0.23	15.0	15.0		4.7	3.6
CP 2 -15-06L	14.0	14.5	1.81	67.5	0.48	15.0	30.0		4.7	7.5
CP 2 -31-06L	14.0	30.0	3.75	67.5	1.00	30.0	30.0		4.7	15.7
CP 2.8-32-06L	24.0	52.0	3.80	67.5	1.00	40.0	40.0		4.7	34.0
CP 5 -31-10L	36.0	81.0	3.75	70.0	1.00	55.0	55.0		5.7	73.0
CP 5 -31-06L	60.0	130.0	3.75	67.5	1.00	55.0	55.0		4.7	64.5
FC SERIES										
FC 0.45- 4-05	0.8	0.22	0.48	67.5	0.125	1.6	3.3	3.3	2.4	All weights below 0.7 g
FC 0.45- 8-05	0.8	0.44	0.97	67.5	0.250	3.3	3.3	4.9	2.4	
FC 0.45-12-05	0.8	0.66	1.46	67.5	0.375	3.3	4.9	4.9	2.4	
FC 0.45-18-05	0.8	0.98	2.18	67.5	0.562	4.9	4.9	6.5	2.4	
FC 0.45-32-05	0.8	1.75	3.88	67.5	1.000	6.5	6.5	8.1	2.4	
FC 0.45-66-05	0.8	3.62	8.00	67.5	2.060	9.7	9.7	11.4	2.4	
FC 0.6- 4-06L	1.1	0.30	0.48	67.5	0.125	2.1	4.1	4.1	2.6	All weights below 0.7 g
FC 0.6- 8-06L	1.1	0.60	0.97	67.5	0.250	4.1	4.1	6.2	2.6	
FC 0.6-12-06L	1.1	0.90	1.46	67.5	0.375	4.1	6.2	6.2	2.6	
FC 0.6-18-06L	1.1	1.35	2.18	67.5	0.562	6.2	6.2	8.2	2.6	
FC 0.6-32-06L	1.1	2.40	3.88	67.5	1.000	8.2	8.2	10.3	2.6	
FC 0.6-66-06L	1.1	5.00	8.00	67.5	2.060	11.2	11.2	14.2	2.6	
FC 0.6- 4-05L	1.4	0.38	0.48	67.5	0.125	2.1	4.1	4.1	2.4	All weights below 0.7 g
FC 0.6- 8-05L	1.4	0.75	0.97	67.5	0.250	4.1	4.1	6.2	2.4	
FC 0.6-12-05L	1.4	1.13	1.46	67.5	0.375	4.1	6.2	6.2	2.4	
FC 0.6-18-05L	1.4	1.69	2.18	67.5	0.562	6.2	6.2	8.2	2.4	
FC 0.6-32-05L	1.4	3.00	3.88	67.5	1.000	8.2	8.2	10.3	2.4	
FC 0.6-66-05L	1.4	6.20	8.00	67.5	2.060	11.2	11.2	14.2	2.4	
FC 0.7- 4-05L	1.9	0.52	0.48	67.5	0.125	2.3	4.6	4.6	2.4	All weights below 0.7 g
FC 0.7- 8-05L	1.9	1.04	0.97	67.5	0.250	4.6	4.6	6.9	2.4	
FC 0.7-12-05L	1.9	1.56	1.46	67.5	0.375	4.6	6.9	6.9	2.4	
FC 0.7-18-05L	1.9	2.34	2.18	67.5	0.562	6.9	6.9	9.2	2.4	
FC 0.7-32-05L	1.9	4.16	3.88	67.5	1.000	9.2	9.2	11.5	2.4	

FC 0.6-4-06L = 0.6 mm x 0.6 mm [illegible]

PARTS LIST

CCD BOARD

Design	Quantity	Manufacture	Part No.	Description
U1	1	EEV	P8602 s/u	385x576 pixel CCD array
R1	1			1K ohms ¼w
R2, R3	2			3.3K ohms ¼w
R4, R6	2		4610X-101-104	9 resistors 100K ohms bussed
C1	1			1uF 25v electrolytic
C2	1			.1uF 25v ceramic
C3, C4	2			10uF 25v electrolytic
Misc.	1			1.9"x1.6" perf. board

PARTS LIST

VIDEO PREAMPLIFIER BOARD

Design	Quantity	Manufacture	Part No.	Description
U1	1	Nat.	LH0032CG	ultra fast fet op amp
R1, R2	2			100 ohms ½w
R3	1	Beckman	68XR10K	10K ohms potentiometer
R4	1			12K ohms ¼w
R5	1			2.7K ohms ¼w
R6	1			820 ohms ¼w
R7	1	Beckman	68XR5K	5K ohms potentiometer
R8	1			10K ohms ¼w
R9, R10	2			560K ohms ¼w
C1, C4	4			10uF 25v electrolytic
C6, C8				
C2, C5	4			.01uF 25v ceramic
C7, C9				
C3	1			4.5 to 20 pF ceramic trimmer
misc	1	ITRES	VBB2	video preamplifier printed circuit board
CNb	1	Amphenol	27-7	female minature coax connector

APPENDIX B

ARRAY COOLING PERFORMANCES

With no water cooling and the camera system in the fast clear mode the different surfaces are listed below:

heat sink	copper block	cooler voltage
46.8°C	21°C	≈ 3.48 volts

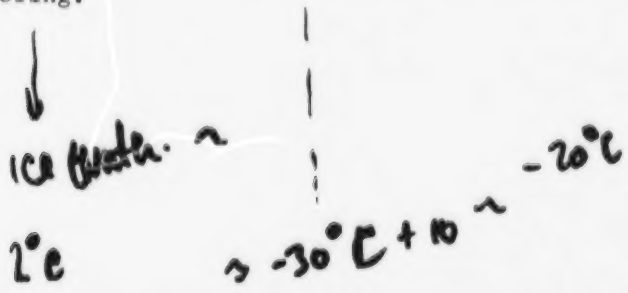
With water cooling and the same setup as above the temperatures are

heat sink	copper block	cooler voltage
32.4°C	9°C	≈ 3.48 volts

Next with the system off and the cooler and water running

heat sink	copper block	cooler voltage
27°C	-4°C	≈ 3.48 volts

Conclude that a larger thermal electric cooler would provide increased cooling.



APPENDIX C

ESTIMATES RE DEVELOPMENT AND MANUFACTURE OF A COMMERCIAL POSITION-SENSITIVE DUAL X-RAY DETECTOR SYSTEM

INTRODUCTION

Key issues addressed in this Appendix are the problem of handling a second detector within the framework of the ITRES CCD readout system; the various possible approaches to reading out the CCD and obtaining data on the number of x-ray events as a function of position (row number) on the array; host computer options and their implications with respect to development and manufacturing costs; anticipated development and retail costs of the most promising approach.

In considering these issues we have taken into account the processing and control capabilities required of the host. We now consider the items outlined above.

PROVIDING FOR A SECOND DETECTOR

There is no problem in providing and driving a second analog board in the camera assembly, which could then clock and read out a second CCD in parallel to the first. The present ITRES system transfers the digitized CCD data over a 12 bit parallel link to a video summation board in the host computer. There would be hardware complications in increasing the link to 24 bits. If, instead, the data were multiplexed on the same bus the bus transfer rate would be cut in half, resulting in a reduction of the readout rate to half its current value. An alternative scenario would be to do a real time subtraction of a threshold value, followed by transmission of a few bits (up to six) from each CCD over the existing parallel link. As described below it may be desireable to accumulate the total counts in each row within the camera assembly itself, thus eliminating the parallel link completely.

READOUT SCENARIOS

Two issues drive our consideration of readout scenarios in opposite directions:

a) minimizing the CCD readout time so that dark current contributions to the total signal are as small as possible, thus simplifying the processing and hopefully eliminating the need for corrections to be applied on an individual pixel basis.

b) providing the best possible dark current correction scheme, thus minimizing the cooling requirements for the CCDs and possibly even permitting room temperature operation.

With the amount of rapid clocking involved in any of the readout scenarios it is likely that some amount of cooling will be required even if only to maintain the array at room temperature. Furthermore, the cost benefits from simplifications to the electronics probably outweigh those from reducing the cooling requirements. Therefore, we consider (a) to be of higher priority than (b).

On-chip charge summation along rows needs to be considered as a means for simplifying the readout electronics. On-chip summation of N rows increases the readout rate by a factor of N in principle, but it also increases the output dark level for the summed pixels (compared to the single pixel level) by a factor of N, making the process neutral as far as the output dark current level is concerned. (see Phase 2 report). However, two other advantages accrue. Effects of charge spreading along the rows are reduced (although spreading in the other direction is not corrected for), and any corrections for dark current nonuniformity are reduced by a factor of N. Charge summation of successive columns (i.e. within rows) is also attractive, but harder to implement electronically, and it provides less than a factor of N gain in readout rate.

TIMING CONSIDERATIONS

Each digitizing cycle of the A-D converter requires 1.0 microseconds; this includes the time to shift the charge once in the horizontal transport register. In addition, each vertical shift of one row into the horizontal transport register requires one microsecond. Therefore, to digitize each pixel in the full array requires 576x385+576 = 220,000 microseconds = .22 sec.

This time can be cut in half by summing two rows at a time into the horizontal register. Charge summing on the output gate can also speed up the readout. With the present electronics horizontal summation can be done with a shifting rate of 4 shifts per microsecond, with an additional overhead of one microsecond each time the summed output is digitized. For example, with 4 pixel summation the readout rate is doubled, with 16 pixel summation it is tripled, and with 64 pixel summation it is nearly quadrupled. Combining summation of two rows and a large ($\geq$ 16) number of columns decreases the readout time to 28 msec. This opens up the possibility of exposure times as short as 150 msec, (5x readout time) which should reduce the dark current to about 400 electrons (4 dn) per pixel at 0 C. At -20C the dark current would be further reduced to about 1 dn (300e) per pixel. Of course, the summed dark value is the important one for evaluating various readout scenarios, as indicated in Table C-1.

TABLE C-1

EXPOSED TIMES AND SUMMED DARK VALUES FOR VARIOUS READOUT SCENARIOS

Summation mode		temp (C)	dark current e/pixel/sec.	exposure time = 10x readout (sec)	dark current per pixel	dark current per summed pixel	
rows,	cols					e	d_n
1	1	0	3000	2.2	6600	6600	70±.2
		-10	1300	2.2	2900	2900	30±.1
		-20	500	2.2	1100	1100	10±.2
2	1	0	3000	1.1	3300	6600	70±.1
		-10	1300	1.1	1400	2900	30±.5
		-20	500	1.1	600	1100	10±.2
2	4	0	3000	.55	1600	13000	130±.1
		-10	1300	.55	700	6000	60±.5
		-20	500	.55	300	2000	20±.2
2	16	0	3000	.14	400	14000	140±.6
		-10	1300	.14	200	6000	60±.3
		-20	500	.14	70	2000	23±.1
3	16	0	3000	.10	300	14000	140±.5
		-10	1300	.10	130	6000	60±.2
		-20	500	.10	50	2000	20±.1

Note the uncertainty values on the summed dark values are standard deviations obtained by taking typical pixel-pixel dark current variability of ±2.4%, dividing by the square root of the number of pixels summed, and multiplying by the summed dn value. These uncertainty values do not include read noise (currently $2\frac{1}{2}$ d_n) or dark noise ($\sqrt{2}$ d_n).

It is clear from the table that an important by product of pixel summation is the reduction of random pixel-to-pixel dark current variations to the point where they become insignificant. If there were no systematic dark current variations (such as would arise from temperature gradients) then dark subtraction could be ignored and a simple threshold could be applied to detect x-ray events. Summing the pixels should also reduce the effects of charge spreading and make individual events more readily detectable. Thus, in the ideal case, x-ray events could be accumulated into a small one-dimensional memory according to row number, within the camera head electronics, from which values could be read into the host via a conventional serial link at the end of each x-ray exposure.

If temperature gradient effects or other systematic pixel non-uniformities cannot be adequately controlled, then it may be necessary to provide another memory array into which are stored sector-dependent threshold values derived automatically from dark current values taken during the run and addressed according to some combination of high order bits from the row and column numbers in the array.

TEMPERATURE CONTROLLER

Although an uncontrolled cooling system is adequate for a laboratory environment, a commercial unit will require some form of active temperature control. Regulation of thermoelectric cooler current based on output of a temperature sensor, probably located at he CCD-copper block interface, is the preferred means of control.

CCD ENCLOSURE

The present CCD package does not incorporate the necessary amount of protection for a production instrument, given that the detector is quite exposed when it is installed in the diffractometer. We therefore would plan to enclose the detector in a metal box except for the end window of the CCD and the side nearest the x-ray tube. This side will be covered by several layers of aluminized mylar multilayer insulation.

CONCLUSIONS

Until more is known about the detailed response of the CCD and its readout system, we cannot pin down definitively many aspects of the design. Nevertheless, some rough estimates can be made of development and production costs based upon reasonable assumptions about the design of the subsystem, as follows:

1. Detector configuration - dual EEV P8602 CCD deep depletion arrays, free from major blemishes, enclosed in metal boxes, with water cooling and upgraded thermoelectric coolers and temperature controllers.
2. MCU - standard ITRES board except modified to use EPROM instead of RAM for program storage, and to use space control bits as necessary to control storage of data in summation memory.
3. Analog Board - dual, one board for each detector.
4. Summation memory - two banks of high speed 16 bit memories to accumulate x-ray counts according to row number using RAM-based look-up table of threshold values loaded over serial link by host.
5. Serial link - standard RS232C serial link to host computer for control and data transfer.

COST ESTIMATES
(based on preceding assumptions)

A. DEVELOPMENT COSTS

1. Design (including necessary bread boarding) and prototype fabrication.

	LABOR (days)			MATERIALS	MISC.
	Sr.Engr.	Engr.	Tech.	($)	($)
a) Complete conceptual design	8	5	3	-	-
b) Detector and improvements	3	2	10	4700	500 (machining)
c) Detector enclosure	3	5	3	200	500 (machining)
d) Temp controller	3	5	7	500	-
e) Dual detector readout system	2	3	5	19775*	-
f) Summation memory & threshold circuit	10	5	10	500	-
g) Host interface (serial link)	3	3	3	250	-
h) Control Software	3	3	15	-	5000 (PC rental)
i) MCU EPROM	3	8	5	200	-
j) Documentation	4	5	5	-	200
2. Assembly and testing	10	10	20	-	-
Total	52	54	86	26125	6200
Labor rates	450	336	242		
Total	23400	18144	20812		

TOTAL COSTS 94,681

* price of off-the-shelf components required for dual detector readout system.

COST ESTIMATES
(based on preceeding assumptions)

B. MANUFACTURING COSTS (Including overhead but not profit or cost recovery)

	LABOR (days)			MATERIALS	MISC. *
	Sr.Engr.	Engr.	Tech.	($)	($)
1. Detector assemblies (2)		4	7	4700	
2. MCU		6	6	420	
3. Analog board (2)		3	3	1940	
4. Summation memory (2)		3	5	700	
5. Temp controller		1	3	350	
6. Assembly and testing	2	5	5	-	
7. Documentation	-	-	-	100	
Total	2	22	29	8210	1290
Labor rates	450	336	242		
Total	900	7392	7018		

TOTAL COST $24,810

* warranty, shipping, etc.